Amendments to the Claims

Please amend the claims as shown below.

1-6. (Canceled)

7. (Currently Amended) A semiconductor device of IGBT comprising:

a top region of a second conductivity type;

a deep region of the second conductivity type;

an intermediate region of a first conductivity type for isolating the top region and the deep region;

a collector region of the first conductivity type contacting with the deep region and being isolated from the intermediate region by the deep region;

an emitter electrode connected with the top region;

a collector electrode connected with the collector region; and

a trench gate facing a portion of the intermediate region via an insulating layer, wherein the portion of the intermediate region facing the trench gate isolates the top region and the deep region, and wherein the trench gate extends along a longitudinal direction in a plan view of the semiconductor device and width of the trench gate varies along the longitudinal direction in a plan view of the semiconductor device.

8. (Currently Amended) [[A]] The semiconductor device according to claim 7,

wherein a plurality of trench gates extending in parallel is provided, and variations of width of trench gates along the longitudinal direction are aligned in phase between adjacent trench gates.

9. (Currently Amended) [[A]] The semiconductor device according to claim 7,

wherein a side wall of the trench gate at a wider width is parallel with a side wall of an adjacent trench gate.

10. (Currently Amended) [[A]] The semiconductor device according to claim 9,

wherein variations of width of each trench gate along the longitudinal direction are repeated cyclically along the longitudinal direction.

11. (Currently Amended) [[A]] The semiconductor device according to claim 10,

wherein a pair comprising a ~~wide trench gate~~wider width and a ~~narrow trench gate~~narrower width is repeated along the longitudinal direction in one trench gate, and total length of the ~~wide trench gate~~ wider width along the longitudinal direction is 30 to 80 % of the total length of the trench gate along the longitudinal direction.

12. (Currently Amended) [[A]] The semiconductor device according to claim 11,

wherein a plurality of trench gates extending in parallel is provided, and variations of width of trench gates along the longitudinal direction are aligned in phase between adjacent trench gates.

13. (Currently Amended) [[A]] The semiconductor device according to claim 12,

wherein width of the intermediate region interposed between adjacent ~~wide~~trench gates at wider width is narrow such that the intermediate region interposed between adjacent ~~wide~~trench gates at wider width becomes a depressed region when on-voltage is not being applied to the trench gates, and the top region is located above the intermediate region interposed between adjacent ~~wide~~ trench gates at wider width.

14. (Currently Amended) [[A]] The semiconductor device according to claim 7,

wherein variations of width of each trench gate along the longitudinal direction are repeated cyclically along the longitudinal direction.

15. (Currently Amended) [[A]] The semiconductor device according to claim 14,

wherein a pair comprising a ~~wide trench gate~~wider width and a ~~narrow trench gate~~narrower width is repeated along the longitudinal direction in one trench gate, and total length of the ~~wide trench gate~~wider width along the longitudinal direction is 30 to 80 % of the total length of the trench gate along the longitudinal direction.

16. (Currently Amended) [[A]] The semiconductor device according to claim 7,

wherein width of the intermediate region interposed between adjacent ~~wide~~ trench gates at wider width is narrow such that the intermediate region interposed between adjacent ~~wide~~ trench gates at wider width becomes a depressed region when on-voltage is not being applied to the trench gates, and the top region is located above the intermediate region interposed between adjacent ~~wide~~ trench gates at wider width.

17. (New) A semiconductor device of IGBT comprising:

a top region of a second conductivity type;

a deep region of the second conductivity type;

an intermediate region of a first conductivity type for isolating the top region and the deep region;

a collector region of the first conductivity type contacting with the deep region and being isolated from the intermediate region by the deep region;

an emitter electrode connected with the top region;

a collector electrode connected with the collector region; and

a trench gate extending through the top region and having a gate electrode, the trench gate further facing a portion of the intermediate region via an insulating layer, wherein the portion of the intermediate region facing the trench gate isolates the top region and the deep region, and wherein the trench gate further extends along a longitudinal direction in a plan view of the semiconductor device and width of the trench gate varies along the longitudinal direction in a plan view of the semiconductor device.